Amendment to the SRIA 2023 Edition

Linking the SRIA with the Chips for Europe Design Platform and Pilot Lines

By themselves research projects contribute partially to resolve societal challenges and to create economic value for Europe. The full leverage of several research projects with significant impact for EU regarding societal and economic impact will happen only if a number of "innovation accelerators" are in place, which will bring the research results to market. Standardisation and regulation, education and training, international cooperation, and research infrastructures are a few of these accelerators.

Discussing those topics is beyond the scope of the ECS SRIA, which is the expression by the industry of its Research and Innovation vision. In essence, the SRIA is designed to be funding instrument agnostic, so that it can constitute the basis of calls for various programmes, such as **Horizon Europe**, **Eureka**, or national initiatives. That being said, some of the accelerators listed above are being set up in the frame of the Chips Act, and we cannot ignore that context. We refer here specifically to the Design Platform and the Pilot Lines included in the Chips for Europe Initiative, which has the objective of supporting and accelerating technological capacity building and innovation in the Union by bridging the gap between the Union's advanced research and innovation capabilities and their industrial exploitation.

The pilot lines are intended to allow companies and academic institutions to perform research on future technologies. By having prototyping capabilities, they allow to assess the feasibility, performance, and reliability of their novel electronic devices, components and modules, or of new manufacturing processes, without affecting ongoing production – in case of industrial pilot lines - or enabling research institutes to showcase their innovations and speed up the time-to-acceptance into the market. SME support via low-volume prototyping is another potential benefit of pilot lines.

Moreover, as pilot lines often involve collaborations between industry partners, research institutions, and academia, they will be fostering the exchange of knowledge, expertise, and best practices in electronics manufacturing to tie these stakeholders more closely together. In this context, pilot lines will also contribute to workforce training, as they will offer hands-on experience and exposure to state-of-the-art technologies and practices. Those collaborations will also pave the way for fast transfer to volume manufacturing ensuring European competitiveness and growth in EU-based share in microelectronics.

While it is outside of the SRIA scope to indicate how these research infrastructures and services should be run, it is important to ensure that their implementation most effectively supports the research needs exposed in the SRIA. To that effect, the following table identifies for the Design Platform and for the Pilot Lines (most likely to be launched as of the time of writing of this amendment to the 2023 ECS SRIA edition) research topics which are expected to be supported by those instruments. Note that the pilot line mechanism is meant to support a large variety of developments, from device manufacturing in semiconductor processes, MEMS, packaging and hybrid integration (SiP), as well as module and system level development. It is therefore expected that other pilot lines, beyond the ones considered here, and focusing on different technologies and different steps in the value chain, could be implemented in later phases.

	Design platform	Advanced 2nm and beyond	FD-SOI	Advanced Packaging and Heterogeneous Integration	Other pilot lines
1.1 Process Technology, Equipment, Materials and Manufacturing		Launching ground for new processes, equipment technologies and materials.	Low-power consumption, radiation hardness, More than Moore app.	Introduce materials and process innovations as well as advanced manufacturing, test and inspection equipment for future AP/HI systems.	
1.2 Components, Modules and Systems Integration	Improve design capabilities to become a closed loop (i.e., to include feedback from the production process and from the field use, respectively) as well as define the new sets of interfaces for the complex integration platforms at die / module / system levels as needed for implementing heterogeneous and chiplet approaches - in particular for ECS applications that will be exposed to demanding and harsh environments (as these ECS are essential for our European backbone industry -automotive, energy, industry, health, ...- and not sufficiently and securely addressed by the worldwide leading players).	Impact of advanced node inflections like backside power distribution networks, forksheet, CFET and 2D material channels 3D heterogeneous integration in chiplet implementation.		Enable enhanced and diversified functionalities (e.g. combined sensing, processing, communication, ...) in small form factor electronic components and systems.	Platforms leading to the scalability of elements enabling connection between the digital and physical worlds (e.g. MEMS, integrated photonics, power electronics, quantum approaches...) in silicon or silicon alternative technologies will provide, together with logical circuitry, additional essential building blocks to be integrated in full fledged electronic systems.
1.3 Embedded software and Beyond		Design Technology Co-Optimisation	Design Technology Co-Optimisation		
1.4 System of Systems		System Technology Co-Optimisation	System Technology Co-Optimisation		
2.1 Edge Computing and Embedded Artificial Intelligence	Provide non-differentiating IPs (I/Os, memory interfaces, etc) Support the Open Source Hardware community in Europe Provide tools for embedded AI, such as tools allowing to quantize and decrease the size of Neural Networks for embedded accelerators.	Drive PPACE (Power - Performance - Area - Cost - Efficiency) improvements for advanced nodes to increase the energy efficiency of computing systems Research PDK's to support managing the increasing complexity of systems.	Energy efficiency, embedded non-volatile memories.	Advanced packaging technologies allow the integration of diverse and specialized components such as processors, GPU/FPGA, memory, sensors and communication chips in a single package. This enables new, more powerful and energy-efficient edge computing, AI and communication solutions in small form factors.	
2.2 Connectivity			* Enable the development of power efficient connectivity solution leveraging European-based semiconductor technology. * Enable the development of innovative connectivity solution at mmW and THz frequencies.	* Enable a European ecosystem that can support heterogeneous integration (multi-die system in a package, advanced assembly capability, advanced substrate manufacturing, etc.) to help European players capture higher value in the connectivity market. * Enable the development of innovative Antenna in package solution at mm-wave and THz frequencies. * Enable a sovereign European packaging ecosystem to secure the supply chain of European semiconductor players (especially in key areas such as space were required manufacturing scale limits the possibility to have acces to Asian OSAT).	
2.3 Architecture and Design : Methods and Tools	Support EDA research and innovation, in particular: - Exponentially increasing design complexity (MC 3) and Increasing Diversity (MC 4), - Sustainability (MC1), - Emerging technologies (MC1), - Increased automation and operability (MC1, MC2, MC3), - Multidisciplinary design (MC4).		Automated application of back-biasing for adjusting power and performance.	Proving ground for new design methods mastering the differences in materials, technologies, and processes that are heterointegrated into a single package.	
2.4 Quality, Reliability, Safety and Cybersecurity	Widen the implementation of Design for X (DfX) besides the design for functionality and performance - in particular for the heterogeneous and chiplet implementations to be used in demanding and harsh environments. Implement 'closed loop design' approaches (= with feedback from manufacturing, testing, ... field use) for manufacturing, testing, reliability, safety, security, repairability, disassembly+reuse, sustainability, etc.			Develop new processes ensuring quality, reliability and safety of heterointegrated chips and systems.	
3.1 Mobility	High Performance automotive SOC for Software Defined Vehicles based on RISC-V (including necessary accelerators and support for automotive bus systems as well as automotive trust-ability concepts).			New generation of environmental sensors (or combined sensors), which simplify and improve object and lane detection, work in difficult (severe) weather conditions and situations (as tunnel exit). Can be supported via Heterogenous integration pilot line, but also via other PL on photonics, quantum sensors. Chiplets will allow for higher functionality and future capabilities to combine processing, sensing, and memory out of different nodes	
3.2 Energy	Energy efficiency is one of the major factors to reduce energy consumption - design for energy efficient devices, process technologies for energy efficient operation and integration and packaging technologies for all the advanced technologies, either logic or power electronics. To manage the demand of the interlinked society for more and more communication and in parallel a sustainable way of operation including fulfilling the transition towards the Green Deal objectives plenty of control and forecasting systems will be required in addition to highly miniaturized, safe, connected and efficient power conversion and distribution systems.				
3.3 Digital Industry				Facilitate advanced, cost-and energy-efficient integrated systems for key application areas.	
3.4 Health					
3.5 Agrifood and Natural Resources	New advanced circuits needed to develop innovative and cost-effective solutions related to the chapter challenges could be designed (through the Design platform programme) and fabricated (through the Pilot lines programme). Examples include sensors for water quality monitoring, GHG emission measurement, plant and soil health.		In agriculture, low cost, highly energy-efficient and self-contained components are essential. They include highly innovative types of sensors related to agriculture and intended to preserve natural resources, highly efficient processors including AI capabilities and long-range RF solutions.	In agricultural devices with a minimal form factor, low power consumption and low cost are essential. The wide variety of devices, related to the multiple applications, requires modular and heterogeneous integration including multiple sensors, advanced processors and multiple RF protocols.	
3.6 Digital Society				Facilitate advanced, cost-and energy-efficient integrated systems for key application areas.	
Long Term Vision		Foundational studies for new processes, equipment technologies and materials.		Establish and nurture advanced packaging and heterointegration expertise in EU. Facilitate and promote AP/HI technology and infrastructure access to foster electronics device and systems innovations.	

The Design Platform, as proposed in the European Chips Act, should also support research in several cross-sectional technologies.

On the one hand, the development of edge AI and embedded computing chips (research areas identified in Chapter 2.1) will be facilitated if the Design Platform covers the following aspects:

- Providing as many non-differentiating IPs (for instance I/O's, memory and communication interfaces, etc.) as possible, allowing to have a one-shop entry for start-up/SMEs and academia to validate into silicon their new architecture ideas in the field of accelerator for IA (at the edge) and embedded systems.
- Supporting the Open Source Hardware community in Europe (e.g. RISC V), where the Design Platform could be linked with Open Source repositories and allowing access of the instances (and the tools to use them, such as compilers, OS and basic middleware).
- One specific topic that the Design Platform should add is to give access to the tools specific for embedded AI, such as tools allowing to quantise and decrease the size of Neural Networks for embedded accelerators (and perhaps to learning databases) so that it will be a single entry for using all those tools in a coherent environment. That will imply certainly to bridge to other platforms either from European projects (NeuroKit2E for example), but perhaps also with non-European repositories such as HuggingFace.

On the other hand, the design platform could be used to investigate many EDA challenges (research areas identified in Chapter 2.3), such as:

- Exponentially increasing design complexity (Major Challenge 3) and diversity (Major Challenge 4):
  - Developing highly complex and heterogeneous systems-on-chip (SoCs) that integrate diverse functionalities.
  - Supporting the design and optimisation of new advanced packaging solutions for complex heterogeneous systems, addressing challenges related to power delivery, thermal management, signal integrity, and testing, etc.
  - Being able to handle the impact of increasing complexity on security, safety, reliability, etc., which requires 'design for trustworthiness'.
  - Design verification: as designs grow larger and more intricate, exhaustive verification becomes increasingly time-consuming and resource-intensive.
  - Design for manufacturability and short time-to-market: EDA tools must evolve to improved yield, reduced variability, and better reliability, to reduce design cycles and facilitate faster design iterations, verification, and optimization, etc.
- Sustainability (Major Challenge 1): EDA tools will need to enable designers to optimise designs for lower power consumption, reduced carbon footprint, and efficient resource utilization.
- Emerging technologies (Major Challenge 1): EDA support for quantum computing, neuromorphic, edge AI, etc. (e.g. EDA tools need to evolve to support quantum circuit design, verification, and optimisation).
- Increased automation and interoperability in the design flow, including for multi-vendor solutions (Major Challenges 1, 2, and 3): increasing complexity has a direct impact on the human effort required to design, validate, test, etc. and on the quality of the final result.
- Multidisciplinary design (Major Challenge 4): ECS require and will require collaboration across various engineering domains, including electrical, mechanical, thermal, and materials engineering. EDA tools must support seamless integration between different design disciplines.

In a nutshell, the Design Platform and the Pilot Lines included in the Chips for Europe Initiative have the potential to offer a valuable research, development and testing ground, a learning environment to advance innovation, enhance manufacturing capabilities, and accelerate the development of cutting-edge electronic products. To make that promise come true, it is of utmost importance that their research roadmaps are established in strong synergy with the contents of the ECS SRIA and that the results are prepared for transfer into volume manufacturing.

The ECS community is positive toward those two instruments under the pre-condition of appropriate involvement of industrial stakeholders in advisory bodies of these two instruments. For the Pilot lines the projects have to be designed to explore new technologies with clear outcome for the European industry at large, and with feedback mechanisms ensuring this is implemented and established over time. For the Design Platform the rules of access and use of the resulting designs (Silicon IP) or chips for companies or laboratories will have to be clearly and carefully crafted to avoid competition distortion.